

ABSTRACT

A clock recovery unit for generating a clock signal corresponding to an asynchronous data signal. The clock recovery unit includes an input port for receiving an incoming data signal; a local oscillator circuit for generating a plurality of clock signals having the same frequency, where the plurality of clock signals are each shifted in phase relative to one another; a sampling unit having a plurality of latches, each of which is clocked by one of the plurality of clock signals generated by the local oscillator circuit, the sampling unit outputting a plurality data samples of the incoming data signal; a data phase alignment unit coupled to the sampling unit, the data phase alignment unit receiving the plurality of data samples as input signals and operative for shifting the phase of the plurality of data samples; a multiplexer circuit coupled to the data phase alignment unit, the multiplexer circuit having a first multiplexer operative for selecting a portion of the plurality of data samples, each of the data samples having a corresponding clock signal, which is one of the plurality of clock signals generated by the local oscillator circuit, the multiplexer circuit having a second multiplexer operative for selecting one of the plurality of clock signals generated by the local oscillator circuit; a phase decoder coupled to the multiplexer circuit, the phase decoder operative for receiving the portion of the plurality of data samples selected by the multiplexer and for generating an output signal indicative of the logic values of the portion of the plurality of the data samples selected by the first multiplexer; and a barrel shifter circuit coupled to the phase decoder, the barrel shifter operative for adjusting the data samples selected by the first multiplexer in accordance with the output signal of the phase decoder.